THSTEP25 Microstepping Stepper Motor Driver	THS Engineering Mechanical & Electro-Mechanical Systems www.thsengineering.com

Datasheet

Last Updated 4/6/2006

Introduction:

THSTEP25 is a bipolar chopper step motor driver based on the Allegro A3977SED chip. Each board drives one axis and is 2.5" X 1.9" in size. **This product is intended for the experienced electronics hobbyist.** It may require some experimenting and modification to work with your particular setup.

Specifications:

Drive type:	2 Phase Bipolar Chopper Microstepping
Step options:	Full, Half, 1/4 and 1/8 Microstepping
Digital Inputs:	Step, Direction, Enable
Digital Outputs:	Home
Chipset:	Allegro A3977SED (44 PLCC SMT)

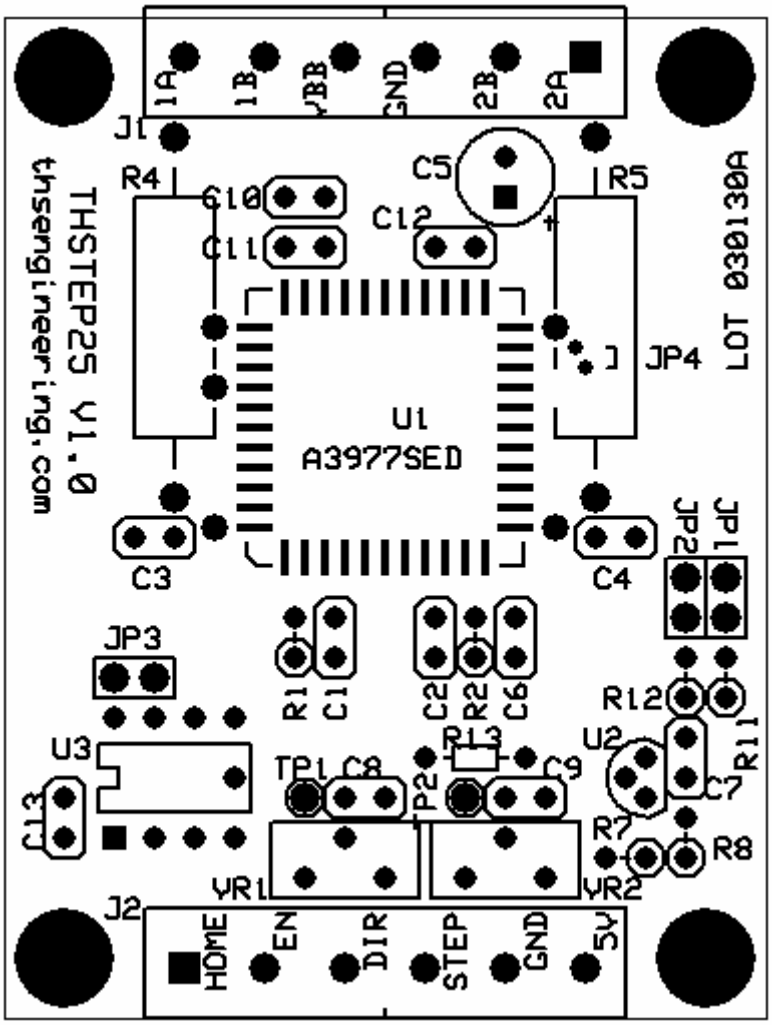
	Recommended	**Absolute Max**
Output Current:	2.0 Amps/phase or less	2.5 Amps/phase
Supply Voltage	12 to 30 VDC	35 VDC

Ordering Info:

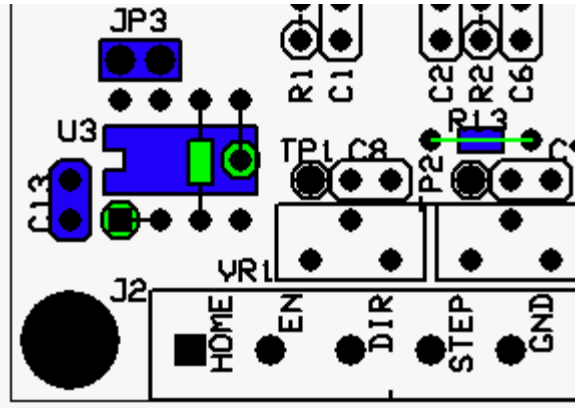
Product #	**Description**
THSTEP25-PCB	Bare PCB only (no parts)
A3977SED	A3977SED IC only
THSTEP25-PS	PCB w/ A3977 soldered on (no other parts)
THSTEP25-PIC	Optional Programmed PIC12F629

Parts Placement:

See website for fully scalable pdf parts placement file.



If not installing the idle current reduction option, omit U3, JP3 and C13. Install a solid wire jumper in place of R13 as shown below. Finally install 3 pull-up resistors if desired.



Bill of Materials:

Ref.	Description	Source	Source P/N	Qty.
PCB	THSTEP25 PCB	THS	THSTEP25-PCB	1
U1	Allegro A3977SED	THS or Newark	A3977SED	1
U2	LM317LZ adj. V reg TO-92	Digi-Key	LM317LZNS-ND	1
U3	PIC Microcontroller[1]	Digi-Key	PIC12F629-I/P	1
U3	8-pin DIP Socket	Digi-Key	A24807-ND	1
J1, J2	2 Position Terminal Block .2"	Digi-Key	ED1975-ND	6
VR1, VR2	BC Multiturn 10k pot	Digi-Key	CT94Y103-ND	2
JP1, JP2, JP3	.025 pin header 2x1	Digi-Key	WM6402-ND	3
JP1, JP2, JP3	Shorting Jumper	Digi-Key	929950-00-ND	3
C1, C2	.001uF (1000pF) Ceramic Cap	Digi-Key	399-4257-ND *	2
C3, C4, C6, C7, C8, C9, C13	.1uF Ceramic Cap	Digi-Key	399-4266-ND *	7
C5	100uF Radial Electrolytic Cap 35V, .1"	Digi-Key	P5165-ND	1
C10, C11, C12	.22uF Ceramic Cap	Digi-Key	399-4289-ND *	3
R1, R2	20k 1/4 Watt 1% Resistor	Digi-Key	20.0KXBK-ND *	2
R4, R5	.2 Ohm "Wire Element" Resistor[2]	Digi-Key	13FR200E-ND *	2
R7	332 Ohm 1/4 Watt 1% Resistor	Digi-Key	332XBK-ND *	1
R8	1.00k 1/4 Watt 1% Resistor	Digi-Key	1.00KXBK-ND *	1
R11, R12, R13	10k 1/4 Watt 5% Resistor	Digi-Key	10KQBK-ND*	3
HX	Optional Heatsink (not yet tested)	Digi-Key	345-1059-ND	1

Notes:
* Starred parts are new Rohs compliant part numbers.

1. PIC Microcontroller must be programmed with THS supplied firmware.

2. Do not use wire*wound* resistors. The current sense resistors must be “low inductance” types.

Sources:
Digi-Key: www.digikey.com
Newark Electronics: www.newark.com

Circuit Description:

A full schematic is available for download from our website: www.thsengineering.com

Reset Input (RESET)	Hard-wired logic HIGH (inactive)
Home Output (HOME)	Brought directly to terminal block
Step Input (STEP)	Brought directly to terminal block (onboard pull-up)
Microstep Select (MS1 and MS2)	Jumpers provided to set each HIGH or LOW
Direction Input (DIR)	Brought directly to terminal block (onboard pull-up)
Internal PWM Current Control	Itrip reference voltage is provide by trimpot VR1 w/ decoupling capacitor. Voltage can be measured on TP1 while adjusting
Fixed Off-Time and RC Blanking	Two 30k resistors and two .001uF capacitors provided (substitute appropriate values for your application)
Charge Pump (CP1 and CP2), Vcp and Vreg	Three .22uF caps provided
Enable Input (ENABLE)	Brought directly to terminal block (onboard pull up)
Sleep Mode (SLEEP)	Hard-wired logic HIGH (inactive)
Percent Fast Decay Input (PFD)	PFD reference voltage is provide by trimpot VR2 w/ decoupling capacitor. Voltage can be measured on TP2 while adjusting
Synchronous Rectification (SR)	Hard-wired logic LOW (active) Cut trace to GND and install JP4 to if using external freewheeling diodes

Layout and Grounding:
Large ground plane provided for low impedance and heat dissipation. 100uF Electrolytic capacitor provided for VBB decoupling

Logic Supply:
A 5 volt DC logic supply is obtained from the stepper supply via the LM317 voltage regulator provided onboard. This regulator was chosen over a fixed regulator because it can tolerate the full rated 35V input of the A3977. Alternately, an external 5 volt supply can be connected to the "5V" pin. **In this**

case the LM317 must not be installed. Note that an external supply must share a common ground with the stepper supply and watch out for ground loops. A .1uF capacitor near the A3977's logic supply input pin provides decoupling.

Idle Current Reduction and Pullups:
U3 is a PIC12F629 programmed with the appropriate firmware. The PIC reduces the Itrip voltage by one half if no STEP activity is detected for 1 second. Installing JP3 prevents current reduction. STEP, DIR and ENABLE take advantage of the built-in pullups on the PIC pins.

If idle current reduction will never be used, you may omit U3, C13, and JP3. Then install three pullup resistors (10k) and a solid jumper wire in place of R13 as shown in the Alternate Parts Placement.

J1 Pinout

Out2A	Connect to winding #2
Out2B	Connect to winding #2
GND	Ground
VBB	Stepper Supply 8-35 VDC
Out1B	Connect to winding #1
Out1A	Connect to winding #1

J2 Pinout

5V	Logic Supply in or out
GND	Ground
Step	Step Input
DIR	Direction Input
EN	Enable Input
HOME	Home Output

Assembly Tips:

Although the A3977 can be soldered using a small soldering iron, we highly recommend reflow soldering.

Make the A3977 the first component that you solder to the board. This is contrary to the usual practice, but that's the only practical way to do it.

If you solder the ceramic capacitors first, you can insert all of them, then flip the board over. The A3977 will act as a spacer between your work table and the

PCB, holding the capacitors in the right position for soldering.

Finally, solder all the remaining components.

Known Issues:

Pin 4 of U3 (the PIC microcontroller) is an unused input pin and was accidentally left unconnected on the revision 1.0 PCB's. Solder a jumper wire from pin 4 to pin 8 so that it is now tied to ground. This has been corrected on rev. 1.1 PCB's.

Startup:

First, install the appropriate microstep mode jumpers.

Microstep Mode	JP1	JP2
Full Step	Install	Install
Half Step	Omit	Install
1/4 Step	Install	Omit
1/8 Step	Omit	Omit

Before powering up for the first time, tie the enable input high. This disables the stepper outputs.

Apply power and check that the 5V supply voltage is corrrect.

Next, install JP3 to disable idle current reduction. Connect a voltmeter between TP1 and GND and adjust the stepper current pot VR1 to the voltage given by the equation:

Vref = 1.6 X (desired current)

Warning: Do not exceed 4 volts unless using Full Step mode ONLY!

Now remove JP3 and verify that the voltage drops to half the set value after about 1 second.

Next, connect a voltmeter between TP2 and GND and adjust the PFD pot VR2 to 2.5 volts.

You may now bring Enable low, applying power to the stepper motor windings.

Firmware Listing:

```
;*****************************************************************
;      Idle Current Reduction Firmware for THSTEP25 v1.0
;      www.thsengineering.com
;
;      Written under MPLAB IDE 6.12.0.0
;      Compiled with MPASM 3.20.08
;            Case Sensitivity DISABLED
;
;      Copyright THS Engineering 2003
;
;      Last Updated on: 2/11/03
;*****************************************************************
;
;      Program Description:
;
;      Initially, the GP4 pin is set high, bypassing R13 and supplying
;      VR1 with 5V.
;
;      The program polls the INT pin interrupt flag in order to detect
;      a rising edge on the STEP signal.  If no activity on the step
;      signal is detected for 1 second, the GP4 pin is set to an input
;      (high-z), allowing the vref volatage to decrease.  GP4 goes high
;      again as soon as the next rising edge is detected on the STEP
;      signal.
;
;      The GP0 pin is also polled.  If GP0 is pulled low, GP4 will
;      stay at 5V.
;
;      Weak pullups are enabled on all pins except GP4.  The DIRECTION
;      and ENABLE signals are connected only to take advantage of the
;      pullups and are not used by the program.
;
;*****************************************************************

       list      p=12f629           ; list directive to define processor
       #include <p12f629.inc>       ; processor specific variable definitions

       errorlevel  -302             ; suppress message 302 from list file

       __CONFIG   _CP_OFF & _CPD_OFF & _BODEN_OFF & _MCLRE_OFF & _WDT_OFF &
_PWRTE_ON & _INTRC_OSC_NOCLKOUT


;***** VARIABLE DEFINITIONS
delay_l                   equ    0x22
delay_h                   equ    0x23




;*****************************************************************
             ORG     0x000        ; processor reset vector
             goto    init         ; go to beginning of program


             ORG     0x00c

init:
             call    0x3FF        ; retrieve factory calibration value
             bsf     status,rp0   ; set file register bank to 1
             movwf   osccal       ; update register with factory cal value
             bcf     status,rp0   ; set file register bank to 0
```

```
            bcf   status,rp0          ;Bank 0
            clrf  gpio                      ;Init GPIO
            movlw 07h                       ;Set GP<2:0> to
            movwf cmcon             ;digital IO
            bsf   status,rp0          ;Bank 1
            movlw b'00111111'   ;Set 0,1,2,3, 4 and 5 as inputs
            movwf trisio                    ;
            bcf   wpu, 4              ;disable wpu on gp4
            bcf   option_reg, not_gppu            ;global enable weak
pullups
            bcf   status,rp0          ;Bank 0



fullcurrent:
            bsf   gpio, 4                   ;set GP4 high
            bsf   status, rp0  ;bank 1
            bcf   trisio, 4           ;make GP4 output
            bcf   status, rp0  ;bank 0

clear:
            bcf   intcon, intf ;clear flag bit
            clrf  delay_l                   ;and delay counters
            clrf  delay_h

loop:
            btfsc  intcon, intf ;check for rising edge on step pin
            goto clear                      ;and clear
            btfss  gpio,0             ;check for jp3 shorted to gnd
            goto clear                      ;and clear

            movlw  d'1'                     ;increment delay counters
            addwf  delay_l, f
            btfsc  status, c
            addwf  delay_h, f
            btfsc  status, c          ;jump to idle when times out
            goto idle                       ;(256x256x16=~1sec)

            nop
            nop
            nop
            nop
            goto loop



idle:
            bsf   status, RP0 ;bank 1
            bsf   trisio, 4    ;make GP4 high-z to activate current
reduction
            bcf   status, RP0 ;bank 0

idleloop:
            btfsc  intcon, intf ;check for rising edge on step pin
            goto fullcurrent
            btfss  gpio,0             ;check for jp3 shorted to gnd
            goto fullcurrent
            goto idleloop


            END
```

Revision History:

2/28/03	Initial pdf version
3/6/03	Corrected error in PIC part number and added rev. history
4/7/03	Changed “VR1” to “VR2” ref. PFD adjustment on page 6. Added suppy Voltage specs to page 1.
6/7/03	Added “Known Issues” section and notes to BOM
4/06/06	Updated BOM to reflect new part numbers.